



17950 Preston Road | Suite 1000 | Dallas, TX 75252

(972) 732-1001

(972) 732-9218 FAX

www.slater-matsil.com

FACSIMILE COVER SHEET

To: Marietta Joyce	Total Pages Sent: 6
Certificate of Corrections Branch	(including cover sheet)
Facsimile Number: 703-308-6672	Transmission Date: June 4, 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ko, et al.	Docket No.:	TSM03-0615
Serial No:	10/729,095	Patent No.:	7,112,495 B2
Date Filed:	December 5, 2003	Date Issued:	September 26, 2006
Title:	Structure and Method of a Strained Channel Transistor and a Second Semiconductor Component in an Integrated Circuit		

Dear Ms. Joyce:

Pursuant to your request, attached please find a copy of the Request for Certificate of Correction and related documents as sent to the USPTO on October 9, 2006 (received by the USPTO on October 13, 2006) for the above-referenced patent.

Please let me know if you require any further documentation to complete this matter.

Best regards,

Natalie Swider
Legal Assistant

Confirmation Respectfully Requested

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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231



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A request for a Certificate of Correction has
been received for U.S. Patent 7112495

TSM03-0615



STEVEN H. SLATER
SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD SUITE 1000
DALLAS, TX 75252

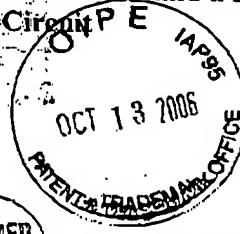
J.P.
lmr



The stamp of the USPTO, placed hereon, acknowledges receipt of:

Patentee:	Ko, et al.	Docket No.:	TSM03-0615
Patent No.:	7,112,495 B2	Issue Date:	September 26, 2006
Serial No:	10/729,095	Art Unit:	2811
Filed:	December 5, 2003	Date Mailed:	October 9, 2006
Title:	Structure and Method of a Strained Channel Transistor and a Second Semiconductor Component in an Integrated Circuit		

Certificate of Mailing via First Class Mail (1 page)
Request for Issuance of Certificate of Correction (1 page)
Certificate of Correction (1 original and 1 copy)
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Ko, *et al.* Docket No.: TSM03-0615
Serial No.: 10/729,095 Filed: December 5, 2003
Patent No.: 7,112,495 B2 Issue Date: September 26, 2006
For: Structure and Method of a Strained Channel Transistor and a Second
Semiconductor Component in an Integrated Circuit

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit: October 9, 2006

I hereby certify that the below listed correspondence is being deposited with the United States Postal Service on the date indicated above as first class mail in an envelope addressed to: Certificate of Corrections Branch, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

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Respectfully submitted,


Michelle Reyes
Legal Assistant

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
Tel: 972-732-1001
Fax: 972-732-9218

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Ko, *et al.* Docket No.: TSM03-0615
Serial No.: 10/729,495 Art Unit: 2811
Patent No.: 7,112,495 B2 Issue Date: September 26, 2006
Filed: December 5, 2003 Examiner: Hung K. Vu
For: Structure and Method of a Strained Channel Transistor and a Second
Semiconductor Component in an Integrated Circuit

Certificate of Corrections Branch
Commissioner for Patents
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Alexandria, VA 22313-1450

Request for Issuance of Certificate of Correction
Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322

Dear Sir:

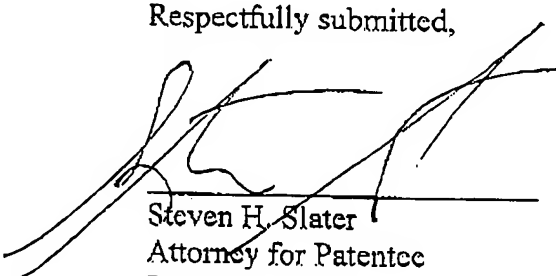
Upon review of the above-identified issued patent, Patentee notes errors in the patent that should be corrected as shown on the attached Certificate of Correction.

The mistakes noted on the attached Certificate of Correction were incurred through the fault of the Patent and Trademark Office. Accordingly, no fee is required.

Patentee respectfully solicits the issuance of the requested Certificate of Correction.

Respectfully submitted,

October 9, 2006
Date


Steven H. Slater
Attorney for Patentee
Reg. No. 35,361

SLATER & MATSIL, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218

PTO/SB/44 (04-05)

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 7,112,495 B2
APPLICATION NO. : 10/729,095
ISSUE DATE : September 26, 2006
INVENTOR(S) : Ko, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 2, Column 1, line 65; delete "6,872,810" insert --6,872,610--
Page 2, Column 2, line 27; delete "TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, vol.49, No. 1, (Jan. 2002), pp.7-14." insert --TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," Symposium On VLSI Technology Digest of Technical Papers, (2002), pp. 96-97.--
Column 5, line 8; delete "patent application" insert --Patent Application--
Column 6, line 24; delete "suicides" insert --silicides--
Column 17, line 2; delete "cobalt suicide" insert --cobalt silicide--
Column 17, line 2; delete "nickel suicide" insert --nickel silicide--
Column 17, line 40; delete "suicide" insert --silicide--
Column 17, line 42; delete "stank" insert --stack--

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application for to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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 Column 5, line 6; delete "patent application" insert --Patent Application--
 Column 6, line 24; delete "sulcides" insert --silicides--
 Column 17, line 2; delete "cobalt suicide" insert --cobalt silicide--
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